Joshua Taylor

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EDUCATION

Carnegie Mellon University **Pittsburgh, PA**
Bachelor of Science in Electrical and Computer Engineering Expected May 2028

- GPA 3.25 / 4.00
- Coursework by Summer 2027: Logic Design and Verification, Introduction to Computer Architecture, Structure and Design of Digital Systems, Electronic Devices and Analog Circuits

Satellite Senior High School **Satellite Beach, FL**
High School Diploma May 2024

- GPA 4.00 (4.61 weighted) / 4.00
- National Merit Scholarship Recipient

WORK & VOLUNTEER EXPERIENCE

Ford Motor Company **Sunrise, FL**
Software Engineering Intern Summer 2026

- Developing internal tooling for Program Managers within the Electronic Platforms team under EV Digital & Design, supporting product development workflows across EV hardware programs
- Contributing to electrical engineering deliverables on embedded/electronic platform systems

BWX Technologies **Melbourne, FL**
IT Architecture & Systems Engineering Intern Summer 2025

- Evaluated Microsoft's CoPilot Studio and Power Automate for production readiness in Government Cloud Controlled High Environment
- Developed AI resume processing tool for HR and AI IT ticket response tool for help desk

PROJECTS

4×4 Systolic MAC Array – Tiny Tapeout ASIC (TTSKY26a)

- Designed a 4×4 systolic matrix MAC in SystemVerilog for a real ASIC tapeout via Tiny Tapeout
  - Full SPI communication interface, FSM-based control unit, and RP2040 firmware
- Validated design on FPGA via UART-driven test harness; resolved accumulator timing and control signal race conditions through python and SystemVerilog constrained random testbenches
- Manages full RTL-to-tapeout flow including TT wrapper integration, yaml_version 6 configuration, and seven-file compile-order

8-Bit RISC-V Processor & Instruction Decoder

- Designed and implemented 8-bit RISC-V single-cycle processor in SystemVerilog on Artix-7 FPGA, including ALU, register file, and control unit with execution state visible via LEDs
- Built complete RISC-V instruction decoder in SystemVerilog covering all six encoding formats
- Includes comprehensive testbench verifying correct field extraction across all instruction types

SKILLS/CERTIFICATIONS

Activities: Robotics Club, Carnegie Tech Radio Club
Languages: C, C#, Python, Java, MATLAB, JSON, SystemVerilog
Platforms: Git, GitHub, Linux, Azure
Tools: Oscilloscope, Signal Generator, Digital Multimeter, DC Power Supply, LTSpice, Vivado, VCS
Certifications: FCC Amateur Radio (Technician Class License KQ4KBW), Cisco CCST Cybersecurity, Autodesk Inventor 2022, Revit 2023, Fusion 2024, Spanish (CEFR B1 Level)